

CLAIMS

1. An imaging device comprising an array of pixels in which, for each pixel, there is provided:
 - 5 a sensor which is sensitive to a variable quantity to be imaged and for outputting a signal representative of the variation in said quantity during an integration period;
 - amplifier means for amplifying the signal from said sensor;
 - a plurality of memory cells for holding sequential samples of the
- 10 amplified signal from the sensor during the integration period; and
- read switch means actuatable to enable the contents of said memory cells to be read out.
2. An imaging device as claimed in claim 1 wherein the sensor, amplifier means, memory cells and read switch means are located within the circuitry of each pixel.
- 15 3. An imaging device as claimed in either one of claims 1 or 2 wherein each memory cell comprises a selection means and a storage means.
4. An imaging device as claimed in claim 3 wherein said selection means is actuated to select that memory cell by a control signal from a common timing circuit.
- 20 5. An imaging device as claimed in claim 4 wherein said timing circuit is such that, during each integration period, at least one memory cell at a time is selected in succession and a sample representative of the instantaneous value of the amplified output signal from the sensor is written to the storage means of the selected memory cell.
- 25 6. An imaging device as claimed in claim 5 wherein the timing circuit acts to write samples throughout the integration period, there being a sufficient number of memory cells that each cell stores a single sample.
7. An imaging circuit as claimed in claim 6 wherein the samples are arranged at evenly spaced time intervals throughout the integration period.
- 30 8. An imaging device as claimed in any one of the preceding claims further comprising write switch means operable to connect the output signal

from said sensor to the memory cells via said amplifier means.

9. An imaging device as claimed in claim 8 wherein said write switch means is operable to energise and de-energise said amplifier means to thereby selectively allow the passage of the output signal of said sensor through the amplifier means to the memory cells.

10. An imaging device as claimed in claim 9 wherein said write switch means comprises a first switch means operable to energise and de-energise said amplifier means as aforesaid, and a second switch means located in the signal path from the output of said amplifier means, and wherein said first and second switch means may or may not be actuated in common.

11. An imaging device as claimed in any one of claims 3 to 10 wherein said timing circuit is further operable, during a read period corresponding with the actuation of said read switch means, to successively read the samples stored within the memory cells.

12. An imaging device as claimed in claim 11 wherein the memory cells are read out on a one-by-one basis.

13. An imaging device as claimed in claim 11 wherein multiple memory cells are read out simultaneously and means are provided for carrying out an analogue operation on the simultaneously read out samples and outputting a resultant signal.

14. An imaging device as claimed in any one of claims 11 to 13 wherein said timing circuit is such as to separate the read period from the integration period, so that they do not overlap.

15. An imaging device as claimed in any one of claims 11 to 13 wherein said timing circuit is such as to overlap the read period and the integration period, and wherein the operations of writing into the individual memory cells and reading from the individual memory cells are time interleaved with one another.

16. An imaging device as claimed in any one of claims 11 to 15 further comprising read reset means for resetting the circuit prior to the commencement of each read period.

17. An imaging device as claimed in claim 16 wherein said reset means is operable to reset the circuit between each reading of a sample stored within a respective memory means.
18. An imaging device as claimed in any one of claims 11 to 17 wherein 5 said read switch means includes a single select switch for sequentially passing the contents of the storage means within respective memory cells, as they are read out, to an output connected to a column bus.
19. An imaging device as claimed in any one of claims 11 to 17 wherein said read switch means comprises a select switch located within each 10 memory cell, wherein said timing means is such as to actuate said select switches to thereby select the memory cells for reading out, and wherein the outputs of said select switches are passed to a common output which is connected to a column bus.
20. An imaging device as claimed in either one of claims 16 or 17 15 wherein said read switch means comprises two select switches, one located between the storage means and the read reset means, and one located between the read reset means and an output connected to a column bus.
21. An imaging device as claimed in any one of the preceding claims 20 wherein said variable quantity is electromagnetic radiation.
22. An imaging device as claimed in claim 21 in which the radiation is visible light.
23. An imaging device as claimed in any one of the preceding claims wherein said sensor is sensitive to charged particles.
24. An imaging device as claimed in any one of the preceding claims 25 wherein said variable quantity is neutron radiation.
25. An imaging device as claimed in any one of the preceding claims wherein said variable quantity is a voltage.
26. An imaging device as claimed in any one of the preceding claims 30 wherein said amplifier means comprises a MOS transistor connected as a source follower.
27. An imaging device as claimed in any one of claims 1 to 25 wherein

said amplifier means is an inverter comprising a pair of MOS transistors.

28. An imaging device as claimed in any one of claims 1 to 25 wherein said amplifier means comprises a charge amplifier.

29. An imaging device as claimed in any one of claims 1 to 25 wherein
5 said amplifier means comprises a differential amplifier having inverting and non-inverting inputs.

30. An imaging device as claimed in claim 29 wherein the output from the sensor is connected to one of said inputs, and a threshold signal is connected to the other of said inputs, the arrangement being such that the
10 amplifier means generates an output only if the input signal exceeds a certain threshold level.

31. An imaging device as claimed in any one of the preceding claims including a further amplifier means for amplifying the signal read out from said memory cells.

15 32. An imaging device as claimed in claims 2 and 31 wherein said further amplifier means is located within the circuitry of each pixel.

33. An imaging device as claimed in claims 18 and 31 or 32 wherein said further amplifier means comprises a single amplifier common to all of said memory cells.

20 34. An imaging device as claimed in claims 19 and 31 or 32 wherein said further amplifier means comprises an amplifier located within each memory cell.

35. An imaging device as claimed in either one of claims 33 or 34 wherein said or each amplifier is constituted by a MOS transistor connected
25 as a source follower.

36. An imaging device as claimed in either one of claims 33 or 34 wherein said or each amplifier comprises a charge amplifier.

37. An imaging device as claimed in any one of the preceding claims wherein said amplifier means is continuously energised during the
30 integration period.